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10/682,134	10/09/2003	David Arnold Luick	ROC920020127US1	1346

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EXAMINER	
MEONSKE, TONIA L	

ART UNIT	PAPER NUMBER
2181	

DATE MAILED: 06/27/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/682,134	LUICK, DAVID ARNOLD	
	Examiner	Art Unit	
	Tonia L. Meonske	2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 April 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17 and 19-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17 and 19-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

FRITZ FLEMING
Supervisory PRIMARY EXAMINER 6/23/2006
GROUP 2100
Art Unit 2181

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claim 9 is objected to because of the following informalities: In line 3, Applicant initially claims a primary latch and then later refers to this primary latch as a first latch in lines 6 and 8. Please change "first" in lines 6 and 8 to "primary". Appropriate correction is required.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-17 and 19-22 are rejected under 35 U.S.C. 102(b) as being anticipated by Terizan, US Patent 4,831,623 (herein after referred to as Terizan).

4. Referring to claim 1, Terizan has taught an integrated circuit comprising:

a. a register file bit comprising:

i. a first latch having a data input and a data output (Figure 1, element 16b, and Figure 1A, elements OP REG 0 and OP REG 1 are all "a first latch". PO MUX, OP MUX 0 and OP MUX 1 are all a "data input" of the first latch. TEST MUX, TEST MUX 0 and TEST MUX 1 are all a "data output" of the first latch.);

ii. a second latch (Figure 1, element 18b, Figure 1A, elements TEST REG 0 and TEST REG 1 are all "a second latch".) having a data input coupled to the data output of the first latch (TRI in Figures 1 and 1A are data inputs for the second latches coupled to the data outputs of the first latch, which are Figure 1, TEST

MUX and Figure 1A, TEST MUX 0 and TEST MUX 1.) and a data output (Figure 1, TR0, Figure 1A, TR), wherein the data input of the second latch is not accessible except through the data output of the first latch (Figure 1A, The data from the first latch (REG 0 and REG 1) is output to a multiplexer (TEST MUX 0 and TEST MUX 1). This data input for the second latch (TEST REG 0 and TEST REG 1) is only accessible through the output of the first latch (TEST MUX 0 and TEST MUX 1));

iii. a feedback path from the data output of the second latch to the data input of the first latch (Figures 1 and 1A, The path from element 18b to element 16b, including element 20b. The path from element TEST REG 0 to element OP REG 0, including element OP MUX 0. The path from element TEST REG 1 to element OP REG 1, including element OP MUX 1.); and

iv. a context switch mechanism that causes the data on the data output of the first latch to be written to the second latch, and that causes the data on the data output of the second latch to be written to the first latch (abstract, Figures 1 and 1A, column 1, line 64-column 2, line 57, Operational data, 16b and OP REG 0, are swapped with test data, 18b and OP REG 1, respectively.).

5. Referring to claim 2, Terizan has taught the integrated circuit of claim 1 as described above, and wherein the context switch mechanism comprises a swap signal coupled to the first latch (Figure 1 and 1A, column 5, lines 1-10, OPER CLK and TEST CLK).

6. Referring to claim 3, Terizan has taught the integrated circuit of claim 1, as described above, and wherein the context switch mechanism comprises a delay element between the data

output of the first latch and the data input of the second latch (Figure 1, element 22b, Figure 1A, elements TEST MUX 0 and TEST MUX 1).

7. Referring to claim 4. Terizan has taught the integrated circuit of claim 1, as described above, and wherein the context switch mechanism comprises a delay element in the feedback path (Figure 1, element 20b, Figure 1A, elements OP MUX 0 and TEST MUX 1).

8. Referring to claim 5, Terizan has taught the integrated circuit of claim 1, as described above, and wherein the context switch mechanism comprises at least one clock signal that latches data on the data input of the first latch to the data output of the first latch (Figures 1 and 1A, OPER CLK) and at least one clock signal that latches data on the data input of the second latch to the data output of the second latch (Figures 1 and 1A, TEST CLK).

9. Referring to claim 6, Terizan has taught the integrated circuit of claim 1, as described above, and further comprising a plurality of write ports on the data input of the first latch (column 4, lines 19-21, OPI parallel inputs).

10. Referring to claim 7, Terizan has taught the integrated circuit of claim 1, as described above, and further comprising a plurality of read ports on the data output of the first latch (column 4, lines 21-22, OPO parallel outputs).

11. Referring to claim 8, Terizan has taught an integrated circuit comprising:

a. a register file bit comprising:

i. a first latch (Figure 1, element 16b, Figure 1A, elements OP REG 0 and OP REG 1) having a data input with a plurality of write ports (column 4, lines 19-21, OPI parallel inputs) and a data output with a plurality of read ports (column 4, lines 21-22, OPO parallel outputs);

ii. a second latch (Figure 1, element 18b, Figure 1A, elements TEST REG 0 and TEST REG 1 are all "a second latch".) having a data input and a data output (TRI in Figures 1 and 1A are data inputs for the second latches coupled to the data outputs of the first latch, which are Figure 1, TEST MUX and Figure 1A, TEST MUX 0 and TEST MUX 1.), wherein the data output of the first latch is coupled to the data input of the second latch through a first delay element (Figures 1 and 1A, The output of 16b is coupled to the input of 18b through element 22b. The output of OP REG 0 is coupled to the input of TEST REG 0 through TEST MUX 0. The output of OP REG 1 is coupled to the input of TEST REG 1 through TEST MUX 1.) and the data input of the second latch is not accessible except through the data output of the first latch (Figure 1A, The data from the first latch (REG 0 and REG 1) is output to a multiplexer (TEST MUX 0 and TEST MUX 1). This data input for the second latch (TEST REG 0 and TEST REG 1) is only accessible through the output of the first latch (TEST MUX 0 and TEST MUX 1));

iii. a feedback path from the data output of the second latch to the data input of the first latch (Figures 1 and 1A, The path from 18b to 16b through 20b. The path from TEST REG 0 to OP REG 0 through OP MUX 0. The path from TEST REG 1 to OP REG 1 through OP MUX 1.), the feedback path including a second delay element (Figure 1 and 1A, element 20b, OP MUX 0 and OP MUX 1); and

iv. a swap signal coupled to the first latch that causes the data on the data output of the first latch to be written to the second latch, and that causes the data

on the data output of the second latch to be written to the first latch (Figures 1 and 1A, OPER CLK and TEST CLK, abstract, column 1, line 64-column 2, line 57, Operational data, 16b, OP REG 0 and OP REG 0, are swapped with test data, 18b, OP REG 1 and OP REG 1, respectively.).

12. Referring to claim 9, Terizan has taught an integrated circuit comprising:

a. a register file bit comprising:

i. a primary latch having a data input and a data output (Figure 1, element 16b, Figure 1A, OP REG 0 and OP REG 1);

ii. a plurality of secondary latches each having a data input and a data output (Figure 1A, TEST REG 0, TEST REG 1);

iii. a feedback path from the data output of the plurality of secondary latches to the data input of the first latch (Figure 1A, The path from TEST REG 0 to OP REG 0 through OP MUX 0. The path from TEST REG 1 to OP REG 1 through OP MUX 1), the feedback path including a data selection mechanism for selecting one data output from the plurality of secondary latches to feed back to the data input of the first latch (FIGURE 1A, OP MUX 0, OP MUX 1); and

iv. a context switch mechanism that causes the data on the data output of the primary latch to be written to a selected one of the plurality of secondary latches, and that causes the data on the data output of the selected one secondary latch to be written to the primary latch (Figures 1 and 1A, OPER CLK and TEST CLK, abstract, column 1, line 64-column 2, line 57, Operational data, 16b, OP REG 0

and OP REG 0, are swapped with test data, 18b, OP REG 1 and OP REG 1, respectively.).

13. Referring to claim 10, Terizan has taught the integrated circuit of claim 9, as described above, and wherein the context switch mechanism comprises a swap signal coupled to the primary latch (Figures 1 and 1A, OPER CLK and TEST CLK).

14. Referring to claim 11, Terizan has taught the integrated circuit of claim 9, as described above, and wherein the context switch mechanism comprises a delay element between the data output of the primary latch and the data inputs of the plurality of secondary latches (Figure 1A, element TEST MUX 0 and TEST MUX 1).

15. Referring to claim 12, Terizan has taught the integrated circuit of claim 9, as described above, and wherein the context switch mechanism comprises a delay element in the feedback path (Figure 1A, OP MUX 0, OP MUX 1).

16. Referring to claim 13, Terizan has taught the integrated circuit of claim 9, as described above, and wherein the context switch mechanism comprises at least one clock signal that latches data on the data input of the primary latch to the data output of the primary latch and at least one clock signal that latches data on the data input of a secondary latch to the data output of the secondary latch (Figure 1A, OPER CLK and TEST CLK).

17. Referring to claim 14, Terizan has taught the integrated circuit of claim 9, as described above, and further comprising a plurality of write ports on the data input of the primary latch (column 4, lines 19-21, OPI parallel inputs).

18. Referring to claim 15, Terizan has taught the integrated circuit of claim 9, as described above, and further comprising a plurality of read ports on the data output of the primary latch (column 4, lines 21-22, OPO parallel outputs).

19. Referring to claim 16, Terizan has taught a method for performing a fast context switch in a register file, the method comprising the steps of: (A) providing a register file bit that stores first and second bit values (Figures 1 and 1A, elements 16 b and 18 b, OP REG 0, OP REG 1, TEST REG 0, TEST REG 1), wherein the register file bit comprises a first latch that stores the first value (Figure 1, element 16b, Figure 1A, elements OP REG 0 and OP REG 1) and a second latch that stored the second value (Figure 1, element 18b, Figure 1A, elements TEST REG 0 and TEST REG 1 are all "a second latch".), the first latch including a plurality of write ports (column 4, lines 19-21, OPI parallel inputs) and a plurality of read ports (column 4, lines 21-22, OPO parallel outputs), the register file bit further including a feedback path that allows the first and second bit values in the first and second latches to be swapped (Figure 1A, The path from TEST REG 0 to OP REG 0 through OP MUX 0. The path from TEST REG 1 to OP REG 1 through OP MUX 1.), wherein the data input of the second latch is not accessible except through the data output of the first latch (Figure 1A, The data from the first latch (REG 0 and REG 1) is output to a multiplexer (TEST MUX 0 and TEST MUX 1). This data input for the second latch (TEST REG 0 and TEST REG 1) is only accessible through the output of the first latch (TEST MUX 0 and TEST MUX 1)); (B) when a context switch is required, swapping the first and second bit values (Figures 1 and 1A, abstract, column 1, line 64-column 2, line 57, Operational data: 16b, OP REG 0 and OP REG 0, are swapped with test data: 18b, OP REG 1 and OP REG 1, respectively.).

20. Referring to claim 17, Terizan has taught the method of claim 16, as described above, and wherein the swapping of the first and second bit values occurs in a single clock cycle (column 5, lines 8-10).

21. Referring to claim 19, Terizan has taught a method for performing a fast context switch in a register file, the method comprising the steps of:

(A) storing a first value in a first latch of the register file (Figures 1 and 1A, element 16b, OP REG 0, and OP REG 1);

(B) moving the first value in the first latch to a second latch (abstract, column 1, line 64-column 2, line 57) wherein the second latch is not accessible except through the first latch (Figure 1A, The data from the first latch (REG 0 and REG 1) is output to a multiplexer (TEST MUX 0 and TEST MUX 1). This data input for the second latch (TEST REG 0 and TEST REG 1) is only accessible through the output of the first latch (TEST MUX 0 and TEST MUX 1));

(C) storing a second value in the first latch of the register file (Figures 1 and 1A, element 18b, TEST REG 0, and TEST REG 1); and

(D) activating a context switch signal that causes the second value in the first latch to be stored in the second latch, and that causes the first value in the second latch to be stored in the first latch (Figures 1 and 1A, OPER CLK and TEST CLK, abstract, column 1, line 64-column 2, line 57, Operational data, 16b, OP REG 0 and OP REG 0, are swapped with test data, 18b, OP REG 1 and OP REG 1, respectively.).

22. Referring to claim 20, Terizan has taught the method of claim 19, as described above, and wherein the activation of the context switch signal in step (D) causes the context switch to occur in a single clock cycle (column 5, lines 8-10).

23. Referring to claim 21, Terizan has taught a method for performing a fast context switch in a register file that includes a primary latch (Figure 1, element 16b, Figure 1A, elements OP REG 0 and OP REG 1) and a plurality of secondary latches (Figure 1, element 18b, Figure 1A, elements TEST REG 0 and TEST REG 1), the method comprising the steps of:

(A) for each of the plurality of secondary latches, performing the steps of:

(A1) storing a value in the primary latch that corresponds to a selected thread

(A2) moving the value in the primary latch to a secondary latch (abstract, column 1, line 64-column 2, line 57);

(B) storing a value in the primary latch that corresponds to an active thread (abstract, column 1, line 64-column 2, line 57);

(C) selecting one of the secondary latches for performing a context switch with the primary latch (abstract, column 1, line 64-column 2, line 57, OP MUX 0 and OP MUX 1); and

(D) performing a context switch between the primary latch and the selected one secondary latch that causes the value in the primary latch to be stored in the selected one secondary latch (abstract, column 1, line 64-column 2, line 57), and that causes the value in the selected one secondary latch to be stored in the primary latch (abstract, column 1, line 64-column 2, line 57).

24. Referring to claim 22, Terizan has taught the method of claim 21, as described above, and wherein the context switch performed in step (D) occurs in a single clock cycle (column 5, lines 8-10).

Response to Arguments

25. Applicant's arguments filed April 20, 2006 have been fully considered but they are not persuasive.

26. On page 12, Applicant argues with respect to claim 1 in essence:

"Terizan does not teach or suggest the second latch is not accessible except through the data output of the first latch"

However, Terizan has taught that the second latch is not accessible except through the data output of the first latch. Applicant is directed to Figure 1A of Terizan. The data from the first latch (REG 0 and REG 1) is output to a multiplexer (TEST MUX 0 and TEST MUX 1). The data input for the second latch (TEST REG 0 and TEST REG 1) is only accessible through the data output of the first latch (TEST MUX 0 and TEST MUX 1). So the second latch (TEST REG 0 and TEST REG 1) is not accessible except through the data output of the first latch (TEST MUX 0 and TEST MUX 1). Also see the rejection to claim 1 above. Therefore this argument is moot.

27. On page 13, Applicant argues in essence:

"Terizan does not teach or suggest a plurality of secondary latches and a data selection mechanism that selects one data output from the plurality of secondary latches to feed back to the primary latch as recited in claim 9."

However, Terizan has taught a plurality of secondary latches and a data selection mechanism that selects one data output from the plurality of secondary latches to feed back to the primary latch. In FIGURE 1A of Terizan, OP MUX 0 selects a data output

from TEST REG 0, to feed back to the primary latch (When B0 is selected.). The output from TEST REG 0 is from the plurality of secondary latches (The secondary latches are TEST REG 0 and TEST REG 1.). Also see the rejection for claim 9 above. Therefore this argument is moot.

Conclusion

28. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

29. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

30. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tonia L. Meonske whose telephone number is (571) 272-4170. The examiner can normally be reached on Monday-Friday, with every other Friday off.

31. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Fritz Fleming can be reached on (571) 272-4145. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

32. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

tlm

Supervisory

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